Sub B1

9. (new) A semiconductor imaging device, comprising:

a) a semiinsulating gallium arsenide (GaAs) substrate;

b) a distributed Bragg reflector mirror epitaxially grown on said semiinsulating GaAs substrate;

c) a first layer of P+ type GaAs deposited on said distributed Bragg reflector mirror;

d) at least one layer of aluminum gallium arsenide (AlGaAs) disposed on said first layer of P+ type GaAs;

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e) an epitaxial layer structure of at least one quantum well of InGaAs having GaAs layers on each either side;

f) a first spacer layer of AlGaAs disposed on said epitaxial layer structure;

g) an N type modulation doped layer of AlGaAs disposed on said first spacer layer;

h) a second spacer layer of AlGaAs disposed on said modulation doped layer;

i) a planar doped layer of P+ type AlGaAs disposed on said second spacer layer;

j) a cladding layer of AlGaAs of modest P type doping disposed on said planar doped layer; and

k) a layer of GaAs of P++ type doping disposed on said cladding layer,

wherein light incident on said semiconductor imaging device causes electrons to leave said at least one quantum well.

10. (new) A semiconductor imaging device according to claim 9, wherein:

said at least one quantum well comprises two or three quantum wells, adjacent of said two or three quantum wells being separated by a GaAs layer.

11. (new) A semiconductor imaging device according to claim 9, wherein:

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said at least one layer of aluminum gallium arsenide (AlGaAs) comprises a P type AlGaAs layer disposed on said first layer of P+ type GaAs and a first layer of undoped AlGaAs disposed on said P type AlGaAs layer.

12. (new) A semiconductor imaging device according to claim 11, wherein:

said at least one layer of aluminum gallium arsenide further comprises a second layer of undoped AlGaAs disposed on said first layer of undoped AlGaAs, said first layer of undoped AlGaAs having a first aluminum content, and said second layer of undoped AlGaAs having a second aluminum content smaller than said first aluminum content.

13. (new) A semiconductor imaging device according to claim 12, wherein:

said first aluminum content is greater than 40% and less than 100%, and said second aluminum content is greater than 10% and less than 30%.

14. (new) A semiconductor imaging device according to claim 13, wherein:

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said first aluminum content is approximately 70% and said second aluminum content is approximately 15%.

15. (new) A semiconductor imaging device according to claim 13, further comprising:

a refractory metal disposed on a portion of said layer of GaAs of P++ type doping, said refractory metal adapted to receive a voltage.

16. (new) A semiconductor imaging device according to claim 9, wherein:

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said semiconductor imaging device is arranged as a pixel with elements i), j) and k) constituting a mesa extending a first horizontal distance, and elements a) through h) extending a second horizontal distance larger than said first horizontal distance.

17. (new) A semiconductor imaging device according to claim 16, further comprising:

a refractory metal disposed on a portion of said mesa layer of GaAs of P++ type doping, said refractory metal adapted to receive a voltage.

18. (new) A semiconductor imaging device according to claim 9, wherein:

said semiconductor imaging device is arranged as a plurality of pixels, each of said plurality of pixels having mesa elements i), j) and k) and separated from an adjacent mesa by a transfer region which does not include elements i), j) and k) and which is implanted with N+ type doping to form a low resistance path between adjacent mesas.

19. (new) A semiconductor imaging device according to claim 18, further comprising:

a refractory metal disposed on a portion of each said mesa atop a layer of GaAs of P++ type doping, said refractory metal adapted to receive a voltage.

20. (new) A semiconductor imaging device according to claim 19, further comprising:

a charge sensitive amplifier coupled to one of said plurality of pixels.

21. (new) A semiconductor imaging device according to claim 20, wherein:

said plurality of pixels comprise a linear array of pixels, said one of said plurality of pixels to which said charge sensitive amplifier is coupled being a last pixel in said linear array, and said charge sensitive amplifier and said linear array together comprise a charge coupled device wherein said plurality of pixels store charges, and wherein said charges are transferred from one pixel to another by an application of clocked voltages to said refractory metal disposed on said mesas.

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22. (new) A semiconductor imaging device according to claim 21, wherein:

said array of pixels is controlled by a clocking scheme chosen from a group consisting of (i) a 1 1/2 phase clocking scheme, (ii) a three phase clocking scheme, (iii) a fully two phase clocking scheme, and (iv) a uni-phase clocking scheme.

23. (new) A semiconductor imaging device according to claim 22, wherein:

said array of pixels is controlled by a 1 1/2 phase clocking scheme, and every other pixel in said linear array of pixels is biased to a constant voltage, and the remaining pixels are clocked with a single phase clock.